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Abstract

Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the implemented technology,

the circuit style and topology, the architecture and at the highest level the algorithms that are being implemented. Multiplier is not only a high delay block but also a major source of power dissipation. This work presents a systematic design methodology for fast and area efficient digital multiplier based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. The performance of this Vedic multiplier is compared with the conventional and fast multipliers being used in practice.

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Index Terms

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Keywords

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bypassing algorithms