Abstract

This project deals with the hardware implementation of the DCT and IDCT algorithm in a more efficient way by the use of CORDIC algorithm. DCT and IDCT are the most widely used transform technique in Digital Image Processing and Digital Signal Processing. This project presents an efficient approach for multiplier less implementation for N-point DCT approximation, which based on coordinate rotation digital computer (CORDIC) algorithm which makes use of shift and add operation for computation. The proposed algorithm is the most popular because of its computational efficiency and structural simplicity. It has advantages such as regular data flow, uniform post scaling factor, arithmetic sequence rotation angels. In this project an N-point DCT is deduced using two N/2-point DCTs by using orthogonal properties of DCT and
IDCT, and also adders are replaced by carry skip adder [1]. Signal flow of 8-point DCT and IDCT CORDIC algorithm are coded and functionality of the design will check using ModelSim simulator. The design will synthesize using Cadence and Xilinx ISE Synthesis tool and the bit file will dumped to a Spartan 3 FPGA kit.

References

- C.-C. Sun, S.-J. Ruan, B. Heyne, and J. Goetze, "Low-power and high quality CORDIC-based loeffler DCT for signal processing," IET Proc. -Circuits, Devices Syst., vol. 1, no. 6, pp. 453–461, 200

Index Terms

Computer Science

Algorithms
Keywords
Coordinate Rotation Digital Computer (cordic) Discrete Cosine Transform (dct)
Fastradix – 2 Algorithm.