Abstract

This paper presents the design of non-sequential phase detector using different XOR gates and compares the results with conventional circuit. Phase detector circuit has been modified using transmission gate logic XOR gate and 4T XNOR gate. The simulation results are focused on accounting the frequency operation and power dissipation of these phase detectors. The results shown in this paper are obtained using 0.35μm CMOS technology on SPICE simulator with 3.3V supply voltage
References


Index Terms

Computer Science

Emerging Trends in Technology

Keywords

Phase Locked Loops (PLL) Are Most Widely Used For Synchronization Of Clock Phase Digital Circuits And High Performance Microprocessor System [1]. The Phase Detector Is The Main Part Of The PLL And There Is An Increasing Demand Of High Frequency Operation PLL. The Action Of Phase Detector Enables The Phase Differences In The Loop To Be Detected And The Resultant Error Voltage To Be Produced. A Phase Detector Can Monitor The Difference Between Input Data Frequency And The Voltage Controlled Oscillator Output And Generate An Up Signal If Input Data Leads The Clock Output Of VCO And A Down If Input Data Lags The Clock [2]. The Most Desirable Feature Of A Phase Detector Is To Have Zero Dead
Zone

Which is responsible for increasing phase noise. Dead zone occurs when the phase detector will not able to detect any phase error when the phase error is present. Various types of phase detector described in literature which are applicable for random data applications. The Hogge’s [3] and Alexander [4] phase detectors have been most widely used. There are some performance limitations in these sequential phase detectors. Here

In this paper modification in non-sequential circuits has been done with transmission gate logic XOR gate and 4T XNOR gate. Further

Different phase detectors are compared with its phase characteristics and power dissipation. Rest of paper is organized as: in section II the structure and operation of phase detector with Complementary XOR Gate in Pass Transistor Logic (cpl) is explained. In section III the modifications have been proposed with XOR and XNOR gates. In section IV the results have been described. Finally the conclusions have been drawn in Section V.