Abstract

Chip multiprocessors are used widely today. The cores in a chip can be homogeneous or heterogeneous. This paper proposes a scheduling algorithm for heterogeneous multiprocessors with multiple functional units of varying speed in each processor. Instructions that can be scheduled in parallel are considered. An optimization function is developed to allocate the processes to the processors that minimize the overall execution time. The proposed model is simulated for a chosen example and verified to give 46% improvement in performance.

Reference

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**Index Terms**

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**Key words**

Chip multiprocessors

Process scheduling