Abstract

In this work, optimized Low power and high speed SRAM architecture based on ten transistor (10T) bit-cell is proposed. This cell obtains low static power and high speed read due to two independent read access mechanisms, which offers cascading of read driver. It also estimates read/write delay, read stability, write stability and compare the result with that of standard 6T, 9T and LP10T SRAM cell. The comparative study based on VDD and Temperature variation using simulation exhibits appreciable improvement in read delay and write SNM.

References


**Index Terms**

Computer Science

Power Electronics
Keywords

Standby Powers, Read Operation Delay, Write Operation Delay, Monte Carlo Simulation and Static Noise Margin.