Comparison of Leakage Power Reduction Techniques in 65nm Technologies

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Authors:
Vikas Singhai, Saima Ayyub, Paresh Rawat

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Abstract

The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk there by evolution of Deep Sub-Micron (DSM) technology; there by the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. Leakage power consumption is one of the major technical problem in DSM in CMOS circuit design. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper comparison of Leakage reduction technique is developed in Cadence Virtuoso in 65nm regime with the combination of stack with sleepy keeper approach with Low Vth & High Vth which reduces the Average Power with respect Basic Nand Gate 29.43%, 39.88%, Force Stack 56.98, 63.01%, sleep transistor with Low Vth & High Vth 13.90, 26.61% & 33.03%, 75.24% with respect to
sleepy Keeper 93.70, 56.01% of Average Power is saved.

References


Index Terms

Computer Science  Power Electronics
Keywords

Leakage Reduction, High speed, Low power, DSM