Abstract

Reversible logic is very lots of in demand for the long term computing technologies as they are known to supply low power dissipation having its applications in Low Power, Quantum Computing, nanotechnology, and Optical Computing. during this paper, we have got given and implemented reversible Wallace signed multiplier circuit in ASIC through changed Baugh-Wooley approach using normal reversible logic gates/cells, based on complementary pass transistor logic and are valid with simulations, a layout vs. schematic check, and a design rule check.

References

2. C. H. Bennett, “Logical reversibility of computation,” IBM Journal of Research and
A Result Analysis of ASIC Design of Reversible Multiplier Circuit


Index Terms

Computer Science
Circuits and Systems

Keywords