

{tag} International Journal of Computer Applications
Foundation of Computer Science (FCS), NY, USA

[Volume 168](#)

-
[Number 13](#)

Year of Publication: 2017

Authors:

Ankita Gupta, Braj Bihari Soni, Puran Gaur

10.5120/ijca2017914233

{bibtex}2017914233.bib{/bibtex}

Abstract

The effects aging of digital circuits are came into the focused due to observations made with several experiments and researchers has start working towards making changes for the improvements in base paper architecture. The integrated device suffers with NBTI and PBTI due to CMOS semiconductor properties and it affects the working of different logic operations and in the same context here we have taken multiplier for consideration and working to develop delay efficient multiplier with aging aware design using adaptive hold logic which is modified in this work to reduce effective delay to speedup circuit logic. The simulation of experiments are conducted in Xilinx IDE 13.1.

References

1. I. C. Lin, Y. H. Cho and Y. M. Yang, "Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 3, pp. 544-556, March 2015.

2. S. Zafar et al., "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO₂/HfO₂ Stacks with FUSI, TiN, Re Gates," 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers., Honolulu, HI, 2006, pp. 23-25.
3. S. Zafar, A. Kumar, E. Gusev and E. Cartier, "Threshold voltage instabilities in high-k gate dielectric stacks," in IEEE Transactions on Device and Materials Reliability, vol. 5, no. 1, pp. 45-64, March 2005.
4. H. I. Yang, S. C. Yang, W. Hwang and C. T. Chuang, "Impacts of NBTI/PBTI on Timing Control Circuits and Degradation Tolerant Design in Nanoscale CMOS SRAM," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 6, pp. 1239-1251, June 2011.
5. R. Vattikonda, Wenping Wang and Yu Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," 2006 43rd ACM/IEEE Design Automation Conference, San Francisco, CA, 2006, pp. 1047-1052.
6. H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-aware flip-flop characterization and design," in Proc. 44th ACM GLSVLSI, 2008, pp. 29–34
7. S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in Proc. ACM/IEEE DAC, Jun. 2007, pp. 370–375.
8. A. Calimera, E. Macii, and M. Poncino, "Design techniques for NBTI-tolerant power-gating architecture," IEEE Trans. Circuits Syst., Exp. Briefs, vol. 59, no. 4, pp. 249–253, Apr. 2012.
9. K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reordering against NBTI-induced performance degradation," in Proc. DATE, 2009, pp. 75–80.
10. Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs," in Proc. ASPDAC, 2011, pp. 603–608.
11. M. Basoglu, M. Orshansky, and M. Erez, "NBTI-aware DVFS: A new approach to saving energy and increasing processor lifetime," in Proc. ACM/IEEE ISLPED, Aug. 2010, pp. 253–258.
12. K.-C. Wu and D. Marculescu, "Aging-aware timing analysis and optimization considering path sensitization," in Proc. DATE, 2011, pp. 1–6.
13. K. Du, P. Varman, and K. Mohanram, "High performance reliable variable latency carry select addition," in Proc. DATE, 2012, pp. 1257–1262.
14. A. K. Verma, P. Brisk, and P. lenne, "Variable latency speculative addition: A new paradigm for arithmetic circuit design," in Proc. DATE, 2008, pp. 1250–1255.
15. D. Baneres, J. Cortadella, and M. Kishinevsky, "Variable-latency design by function speculation," in Proc. DATE, 2009, pp. 1704–1709.
16. Y.-S. Su, D.-C. Wang, S.-C. Chang, and M. Marek-Sadowska, "Performance" optimization using variable-latency design style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 10, pp. 1874–1883, Oct. 2011.

Index Terms

Computer Science

Circuits and Systems

Keywords

Adaptive hold logic, row bypassing, column bypassing, Multiplier, Aging Effect, NBTI, PBTI, Delay Efficient