Abstract

Power consumption is an important issue in today’s world. Growing market of electronic system replaces the conventional digital system by reversible logic circuit to solve the problem of loss of information which was dissipated in the form of heat in irreversible circuit. As digital system implemented using AND and OR gates dissipates major amount of energy in the form of bit erased during logical operation where according to R. Landuer and Bennett concludes that one bit energy loss equalize the information loss in the form of KTln2 joules per bit per cycle unavoidable heat dissipation. Thus in this project, garbage free reversible computing system investigated from abstract design to physical gate level implementation. This proposed design is compared in terms of gate count, quantum cost and propagation delay. This reversible CPU designed using Feynman gate, Peres gate, Toffoli gate and DKG gate. It is synthesized on Xilinx 6.1i ISE and simulation result verifies the correction and modification of proposed design. Survey of this paper is based on types of reversible gates and four parameter that is gate count, ancilla input, garbage output, and quantum cost. This survey had great impact on quantum computing, nanotechnology, QCA, and low power VLSI.
References


**Index Terms**

Computer Science  
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**Keywords**

Reversible gates, Central Processing Unit (CPU), Garbage output, gate count, and quantum cost.