Abstract

The AMBA Advanced high performance bus (AHB) protocol design acts as an interface between two different IP cores. In this work initially the investigation on the AHB is carried out and the basic commands and its working are identified based on which the signal flow diagram and the specifications are developed for designing the AMBA-AHB using VHDL. In this paper
we propose the design and implementation of a flexible arbiter scheme for the AHB bus matrix based on burst operation. Basically, AHB burst operation is that a sequence of operation happens with respect to the size given and it supports only three burst sizes. The size is acting as one of the input to the master during the burst operation and after each burst operation, the master or slave will go to the IDLE stage. The AHB design contains basic blocks such as master and slave and the working of these blocks based on arbitration scheme. According to arbitration scheme only one master can Access the bus at any one time. Multiplexer and Decoders are used to selects the appropriate signals between master and slaves that are involved in the transfer. This AMBA-AHB protocol can be adopted in all the applications provided the design should be an AHB compliant.

Reference

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Index Terms
Key words

AHB busmatrix    Arbiter    System on Chip

FSM for master and slave

Master and slave side arbitration

IP

VHDL