Abstract

Analog and mixed architectures design with high performance suffered from many difficulties due to low power supply, consumption, and the trend toward reducing the size of the circuit. Currently, these performances are considered one of the main constraints in analog design. Characterized and designed of mixed circuits such as Charge Pump-Phase Locked Loops (CP-PLLs) is a challenge in mixed-signal integrated circuits design. In this paper, an effective CMOS CP-PLLs architecture for RF applications that operates at a low power supply 2V into a large range frequency is presented. The proposed CP-PLLs architecture has two novel design blocks which are respectively Phase Frequency Detector (PFD) and Voltage Controlled Oscillator (VCO). The key advantage of the two novel designs is that uses a simple circuit, provide more stable operation compared with other structures recently used and reduce the chip area overhead. Also, the novel VCO design solved the problems caused by recent structures. The CP-PLLs is designed and evaluated using electrical simulator tolls (ADS) with 0. 35?m AMS CMOS technology. Simulations results show a good performance and the effectiveness of the proposed structure.
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Index Terms

Computer Science  Circuits And Systems

Keywords

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