Abstract

Network on Chips are a method of interconnecting Processing Elements, such as processors and communication controllers, through a high scalability interconnect architecture. Planning and implementing NoCs is a complex task, and simulating them at the RTL level is time consuming which has motivated the implementation of a big number of cycle accurate and behavioral simulators. In this paper, we join the effort of NoC simulation platform implementation and we introduce a high level NoC simulation platform that is based on Mathworks Simulink and the SimEvents discrete event simulation engine. We, then, model a 2D and a 3D mesh NoCs using this method and we evaluate their performances. The obtained results are, then, validated using the booksim2 cycle accurate NoC simulator.

References

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Index Terms

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Keywords

2D, 3D NoC, Latency, Throughput