Design Analysis of Low Drop-Out Voltage Regulator with Current Buffer Compensation

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Abstract

A Voltage Regulator which can drive on very small differential voltage is projected called Low Drop-Out Voltage Regulator (LDO). It consist of Trans-Conductance Amplifier as an Error Amplifier (EA) in accordance with its current buffer compensation scheme. This Error Amplifier (EA) provides boost in the gain, enhanced the closed-loop bandwidth of the Low Drop-Out Voltage Regulator. While the current buffer compensation scheme using a current feedback amplifier, offers low output impedance, due to the huge gate capacitance of the pass transistor of the LDO regulator to high frequency. Also in Error Amplifier a Power Noise Cancellation Mechanism is formed which reduces the size of the Pass transistor. Due to this reduced and compact area of the proposed LDO regulator leads to an area efficient chip which finds its applications for wide range of portable electronics. Topographies of proposed LDO are experimentally tested on Cadence in a standard of 45nm technology. This proposal exploits a cascode current amplifier where a high threshold pMOS operated in the sub-threshold region, is responsible to lift the gain and produce the anticipated output voltage. The outcomes show that this circuit functions properly while there is reduction in power consumption by 43.64% and
improvement in regulated Voltage output by 52%.

References


Index Terms
Computer Science                                       Power Systems

Keywords

Low Drop-Out Voltage Regulator, Trans-conductance Amplifier, Programmable Circuit, Cadence.